DC-DC CONVERTER

CROSS-REFERENCE TO RELATED APPLICATION

This application is based upon and claims the benefit of priority from Japanese Patent Application No. 2015-052570, filed March 16, 2015; the entire contents of which are incorporated herein by reference.

FIELD

An embodiment described herein relates generally to a DC-DC converter.

BACKGROUND

In a DC-DC converter, a high side transistor and a low side transistor are alternately switched and thereby an inductor is driven. After electric energy is converted into magnetic energy without loss, the magnetic energy is again converted into electric energy by an output capacitor, and thus a conversion of a DC voltage level is performed.

If an NMOS transistor is used as the high side transistor, a voltage higher than an input voltage is applied to a gate control circuit that controls the gate of the high side transistor, and thus a bootstrap capacitor is usually connected between two power supplying nodes of the gate control circuit.

In a light load state in which a load of the DC-DC converter is small, the high side transistor and the low side transistor perform an intermittent operation, and thereby reducing power consumption is generally performed. In this case, it is considered that a charged voltage of a bootstrap capacitor is monitored such that the charged voltage of the bootstrap capacitor is not decreased too much, and if the charged voltage is equal to or lower than a predetermined voltage which is set in advance, the low side transistor is forcibly turned on, thereby charging the bootstrap capacitor again. However, during the intermittent operation, turning on the low side transistor regardless of being in the light load state increases a wasteful power consumption.

An example of related art includes JP-A-2014-23269.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a circuit diagram of a DC-DC converter according to an embodiment.

FIG. 2 is a timing diagram at the time of a normal operation of the DC-DC converter of FIG. 1.

FIG. 3 is a timing diagram at the time of a light load and when an input voltage is higher than an output voltage by a first voltage.

FIG. 4 is a timing diagram at the time of a light load and when an input voltage is equal to or lower than an output voltage by a first voltage.

DETAILED DESCRIPTION

[0006]

An embodiment provides a DC-Dc converter that can charge a bootstrap capacitor with a low power consumption at the time of a light load;

[0007]

[0009]

Hereinafter, an embodiment will be described with reference to the drawings. The following embodiment will be described with a focus on a characteristic configuration and an operation of a DC-DC converter, but configurations and operations which are omitted in the following description may exist in the DC-DC converter. However, the configurations and operations which are omitted are also included in the scope of the present embodiment.

[0010]

FIG. 1 is a circuit diagram of a DC-Dc converter 1 according to an embodiment. The DC-Dc converter 1 of FIG. 1 includes a bootstrap capacitor Cboot, a high side transistor (first transistor) Q1, a low side transistor (second transistor) Q2, a first gate control circuit 2, a second gate control circuit 3, a low voltage detection circuit (third detection circuit) 4, a voltage difference detection circuit (first detection circuit) 5, a light load determination circuit (determination circuit) 6, a first charging control circuit 7, an error voltage detection circuit (second detection circuit) 8, and a second charging control circuit 9.

[0011]

The high side transistor Q1 is connected between a node n1 of an input voltage Vin of the DC-Dc converter 1 and a terminal LX of an inductor L1. The high side transistor Q1 is, for example, an NMOS transistor. By configuring the high side transistor Q1 by using an NMOS transistor, an ON resistance can be reduced and efficiency is increased, compared to configuring the high side transistor Q1 by using a PMOS transistor. However, in order to completely turn on an NMOS transistor, a gate-source voltage has to be large, and a gate voltage of the NMOS transistor needs to be higher than a drain voltage thereof. Since the drain voltage is the input voltage Vin of the DC-Dc converter 1, it is necessary to generate a gate voltage higher than the input voltage Vin. Therefore, the DC-Dc converter 1 of FIG. 1 is configured, in such a manner that the bootstrap capacitor Cboot is connected between a high side power supply node (first power supplying node) n2 and a high side ground node (second power supplying node) n3 of the first gate control circuit 2 that controls a gate voltage of the high side transistor Q1, and a power supply higher than the input voltage Vin is supplied to the first gate control circuit 2.

[0012]

The first gate control circuit 2 includes a level shift circuit 11, and an inverter IV1 that inverts an output voltage of the level shift circuit 11 and outputs the inverted voltage. An output voltage of the inverter IV1 becomes the gate voltage of the high side transistor Q1.

[0013]

The low side transistor Q2 is connected between the terminal LX of the inductor L1 and a low side ground node (reference voltage node) GND. The low side transistor Q2 is, for example, an NMOS transistor.

[0014]

The second gate control circuit 3 is connected to the gate of the low side transistor Q2. The second gate control circuit 3 includes a logic operation unit 12, a signal processing unit 13, and an inverter IV2. The logic operation unit 12 will be described later. The signal processing unit 13 generates control signals for both of the first gate control circuit 2 and the second gate control circuit 3. The inverter IV2 inverts the control signal and generates a gate voltage of the low side transistor Q2. In addition, the control signal for the first gate control circuit 2 which is generated by the signal processing unit 13 is level-shifted by the level shift circuit 11 included in the first gate control circuit 2, and thereafter is input to the inverter IV1.

[0015]

An output terminal OUT of the DC-Dc converter 1 which outputs an output voltage Vout is connected to the other terminal of the inductor L1, and an output capacitor Cout and a load Rload are connected between the output terminal OUT and the low side ground node GND. It is assumed that a size of the load Rload is variously changed.

[0016]

The voltage difference detection circuit 5 detects whether or not a voltage difference between the input voltage Vin and the output voltage Vout of the DC-DC converter 1 is equal to or lower than a first voltage, and outputs a detection signal that indicates whether to be equal to or lower than the first voltage or not. The first voltage is, for example, 5 V. The detection signal that is output from the voltage difference detection circuit 5 is supplied to the other input node of the logic operation unit 12. For example, the detection signal becomes a high potential, if the voltage difference is equal to or lower than the first voltage.

[0017]

The low voltage detection circuit 4 is connected between both electrodes of the bootstrap capacitor Cboot, detects whether or not a charged voltage of the bootstrap capacitor Cboot is equal to or lower than a second voltage, and supplies the detection signal that indicates whether to be equal to or lower than the second voltage or not to one input node of the logic operation unit 12 described above. For example, if the charged voltage of the bootstrap capacitor Cboot is equal to or lower than the second voltage, the low voltage detection circuit 4 makes the detection signal become a high potential. Here, the second voltage is a voltage that is required for recharging of the bootstrap capacitor Cboot, and more specifically, is a voltage that does not guarantee an ON operation of the high side transistor Q1, if the bootstrap capacitor Cboot is not recharged. Actually, the second voltage is a voltage that is determined by characteristics of the high side transistor Q1, or the like.

[0018]

The logic operation unit 12 is, for example, an AND gate that outputs a logical product signal of two input nodes. An output of the logic operation unit 12 becomes a high potential, when a voltage difference between the input voltage Vin and the output voltage Vout of the DC-Dc converter 1 is equal to or lower than the first voltage, and the charged voltage of the bootstrap capacitor Cboot is equal to or lower than the second voltage. The output signal of the logic operation unit 12 is input to the signal processing unit 13.

[0019]

The logic operation unit 12 need not be configured by an AND gate. The logic operation unit 12 may be configured by combining various types of logic gates.

[0020]

The error voltage detection circuit 8 detects an error voltage that indicates a voltage difference between the voltage Vout on the other terminal side of the inductor L1 and a reference output voltage that is set in advance. If the error voltage is small, the error voltage indicates that the output voltage Vout of the DC-Dc converter 1 is close to the reference output voltage, and it is possible to determine that the load Rload is light.

[0021]

The light load determination circuit 6 determines whether to be in the light load state indicating that the load Rload is light or not, based on the error voltage. More specifically, the light load determination circuit 6 determines that a load is in the light load state, if the error voltage is equal to or lower than a predetermined voltage that is set in advance.

[0022]

The signal processing unit 13 generates a control signal for the high side transistor Q1 and a control signal for the low side transistor Q2, based on a voltage on the one terminal LX side of the inductor L1, the output signal of the logic operation unit 12, the output signal of the light load determination circuit 6, and the error voltage. For example, if it is determined that a load is in a light load state by the light load determination circuit 6, the signal processing unit 13 generate a control signal that turns off together the high side transistor Q1 and the low side transistor Q2.

[0023]

In this way, at the time of a light load, the high side transistor Q1 and the low side transistor Q2 are turned off together, and thereby power consumption is reduced. However, if the charged voltage of the bootstrap capacitor Cboot is lowered, charging of the bootstrap capacitor Cboot is performed, using the first charging control circuit 7 or the second charging control circuit 9, as will be described later. The second charging control circuit 9 instantaneously turns on the low side transistor Q2.

[0024]

If it is determined that the voltage difference is higher than the first voltage by the voltage difference detection circuit 5, the first charging control circuit 7 performs charging of a capacitor in a state in which the second transistor is turned off.

[0025]

The first charging control circuit 7 includes a current source 21, a Zener diode (constant voltage source) 22, and a third transistor Q3, as a more specific example. The current source 21 is connected between an application node of the input voltage Vin and the gate of the third transistor Q3. The Zener diode 22 is connected between the gate of the third transistor Q3 and the high side ground node n3. That is, the current source 21 and the Zener diode 22 are connected in series between the application node of the input voltage Vin and the high side ground node n3. The third transistor Q3 is, for example, an NMOS transistor, a drain thereof is connected to the application node of the input voltage Vin, and a source thereof is connected to the high side power supply node n2. As will be described later, the third transistor Q3 operates at an active region. If a voltage difference between the application node of the input voltage Vin and the high side power supply node n2 is equal to or higher than a predetermined voltage, the third transistor Q3 makes a current flow from the application node of the input voltage Vin to the high side power supply node n2, and thereby charging of the bootstrap capacitor Cboot is performed.

[0026]

The second charging control circuit 9 is connected between the high side power supply node n2 and the low side ground node GND. The second charging control circuit 9 charges a capacitor when the low side transistor Q2 is turned on. The second charging control circuit 9 includes a diode D1 and a DC power supply 23 which are connected in series between the high side power supply node n2 and the low side ground node GND. An anode of the diode D1 is connected to the DC power supply 23, and a cathode of the diode D1 is connected to the high side power supply node n2.

[0027]

A voltage level Vs1 of the DC power supply 23 is higher than a voltage level Vcboot1+Vgs of the Zener diode 22. According to this, if the charged voltage Vcboot1 of the bootstrap capacitor Cboot is decreased to a voltage level of the Zener diode 22, recharging of the bootstrap capacitor Cboot is performed by using the first charging control circuit 7.

[0028]

FIG. 2 is a timing diagram at the time of a normal operation of the DC-Dc converter 1 of FIG. 1. Here, the normal operation means that the load Rload is heavier than that in a light load state.

[0029]

FIG. 2 illustrates an example in which the bootstrap capacitor Cboot is charged previously, in a time t1. In times t1 to t2, the high side transistor Q1 is turned on, and the low side transistor Q2 is turned off. According to this, a voltage VLX on the one terminal LX side of the inductor L1 is increased up to approximately the same potential as the input voltage Vin, and a current ILX flowing through the inductor L1 is linearly increased. In times t1 to t2, charging of the bootstrap capacitor Cboot is not performed, and thus, the charged voltage of the bootstrap capacitor Cboot is gradually decreased.

[0030]

Times t2 to t3 are a dead time in which both the high side transistor Q1 and the low side transistor Q2 are turned off. The reason why the dead time is provided is to prevent a penetration current. In this period, a voltage on the one terminal LX side of the inductor L1 is sharply decreased, and in addition, the charged voltage of the bootstrap capacitor Cboot is also graduaaly decreased. The inductor L1 cannot switch sharply the direction of a current, and thus a current is gradually decreased after the time t2.

[0031]

In times t3 to t4, the high side transistor is turned off, and the low side transistor Q2 is turned on. According to this, a voltage on the one terminal LX side of the inductor L1 goes to a ground level (for example, 0 V). The current flowing through the inductor L1 is decreased gradually and continuously. If the low side transistor Q2 is turned on, a voltage of the high side power supply node n2 that is the one terminal side of the bootstrap capacitor Cboot is also decreased, under the influence of the voltage on the one terminal LX side of the inductor L1 that goes to the ground level, by a law of charge conservation. According to this, charging of the bootstrap capacitor Cboot is performed through the second charging control circuit 9, and thereby the bootstrap capacitor Cboot enters a fully charged state. Therefore the charged voltage of the bootstrap capacitor Cboot is approximately constant.

[0032]

Times t4 to t5 are dead times in which both the high side transistor Q1 and the low side transistor Q2 are turned off. In this period, the charged voltage of the bootstrap capacitor Cboot is gradually decreased. Thereafter, after a time t5, the same operations as in times t1 to t5 are repeated.

[0033]

In this way, at a normal operation, the DC-Dc converter 1 of FIG. 1 alternately turns on the high side transistor Q1 and the low side transistor Q2, and generates the output voltage Vout with a voltage level different from the input voltage Vin. By controlling a ratio of an ON period of the high side transistor Q1 and the low side transistor Q2, the voltage level of the output voltage Vout can be adjusted.

[0034]

FIG. 3 is a timing diagram at the time of a light load and when a potential difference between the input voltage Vin and the output voltage Vout is higher than the first voltage. In this case, the voltage difference detection circuit 5 outputs a detection signal with a low potential which indicates the input voltage Vin is higher than the output voltage Vout by the first voltage.

[0035]

In times t11 to t14, the same operations as in the time t1 to t4 of FIG. 2 are performed. In a time point of the time t14, if it is determined by the light load determination circuit 6 that a load is a light load, after the time t14, the high side transistor Q1 and the low side transistor Q2 are turned off together. According to this, the charged voltage of the bootstrap capacitor Cboot is gradually decreased.

[0036]

In a time point of the time t14, the one terminal LX of the inductor L1 has a high impedance, but the other terminal side of the inductor L1 has the output voltage Vout according to the charged voltage of an output capacitor Cout. For this reason, a voltage on the one terminal LX side of the inductor L1 vibrates greatly in the time t14, and a vibration amplitude thereof is gradually decreased, and eventually becomes the same potential as the output voltage Vout on the other terminal side.

[0037]

At a time t15, if the charged voltage of the bootstrap capacitor Cboot is decreased to a predetermined voltage Vboot1, the voltage of the high side power supply node n2 is decreased, a gate-source voltage of the third transistor Q3 in the first charging control circuit 7 is increased, a current flows from the application node of the input voltage Vin to the high side power supply node n2 via the third transistor Q3, and charging of the bootstrap capacitor Cboot is performed. The third transistor Q3 operates at an active region, not at a saturation region. Thus, from the time t15 to time t16 in which the high side transistor Q1 is turned on, the first charging control circuit 7 continuously charges the bootstrap capacitor Cboot, and the voltage of the high side power supply node n2 is maintained as approximately the voltage Vboot1. After the time t16, the same operations as the operations in the times t11 to t16 are repeated.

[0038]

The first charging control circuit 7 continuously supplies a slight charging current to the bootstrap capacitor Cboot via the third transistor Q3, and performs charging of the bootstrap capacitor Cboot. That is, the first charging control circuit 7 simply makes a current with an amount necessary for charging the bootstrap capacitor Cboot flow, and it is possible to further reduce power consumption than charging the bootstrap capacitor Cboot by turning on the low side transistor Q2.

[0039]

In this way, in the present embodiment, at the time of a light load and when a voltage difference between the input voltage Vin and the output voltage Vout is higher than the first voltage, charging of the bootstrap capacitor Cboot is performed by using the first charging control circuit 7, in a state in which the low side transistor Q2 is turned off.

[0040]

FIG. 4 is a timing diagram at the time of a light load and when a voltage difference between the input voltage Vin and the output voltage Vout is equal to or lower than the first voltage. In this case, the voltage difference detection circuit 5 outputs a detection signal of a high potential which indicates that a voltage difference between the input voltage Vin and the output voltage Vout is equal to or lower than the first voltage. In this state, if the low voltage detection circuit 4 detects that the charged voltage of the bootstrap capacitor Cboot is equal to or lower than a second voltage, an output of the logic operation unit 12 becomes high. According to this, the signal processing unit 13 releases fixed OFF of the low side transistor Q2.

[0041]

In times t21 to t24, the same operations as in the times t11 to t14 are performed. In the time t24, if the high side transistor Q1 and the low side transistor Q2 are turned off together, the charged voltage of the bootstrap capacitor Cboot is gradually decreased. Thereafter, in the time t25, the low voltage detection circuit 4 detects that the charged voltage of the bootstrap capacitor Cboot is equal to or lower than the second voltage. According to this, the output of the logic operation unit 12 goes to a high potential. At this time, if it is determined that the light load determination circuit 6 is also in the light load state, the signal processing unit 13 outputs a control signal of a low potential. This control signal is inverted by an inverter, and the gate of the low side transistor Q2 goes to a high potential. Thus, the low side transistor Q2 is turned on just for a moment, and the voltage VLX on the one terminal LX side of the inductor L1 is decreased. By a law of charge conservation, a voltage on one terminal side of the bootstrap capacitor Cboot, that is, a voltage on the high side power supply node n2 is also decreased. Thus, charging of the bootstrap capacitor Cboot is performed by a voltage that is output from the DC power supply 23 via the diode D1, which are included in the second charging control circuit 9. According to this, the charged voltage of the bootstrap capacitor Cboot is rapidly increased. Thereafter, after the time t25, the operations in times t21 to t25 are repeated.

[0042]

ON switching of the low side transistor Q2 in the time t25 is made due to the charging of the bootstrap capacitor Cboot, and turning-on of the low side transistor Q2 is made just for a moment. If a period in which the low side transistor Q2 is turned on is lengthened, a large current flows from the inductor L1 to the low side transistor Q2 side, and the output voltage Vout is also decreased.

[0043]

In addition, when a voltage difference between the input voltage Vin and the output voltage Vout is equal to or lower than the first voltage, the bootstrap capacitor Cboot is not charged by the first charging control circuit 7, and this is because there is a possibility that, when the voltage difference between the input voltage Vin and the output voltage Vout is small, the voltage of the high side power supply node n2 is almost not decreased, with respect to the voltage of the node n1 of the input voltage Vin, a source voltage is almost not decreased with respect to a gate voltage of the third transistor Q3 in the second charging control circuit 9, and a sufficient charging current does not flow into the bootstrap capacitor Cboot via the third transistor Q3.

[0044]

In this way, in the present embodiment, at the time of a light load and when the input voltage Vin is higher than the output voltage Vout by the first voltage, if the charged voltage of the bootstrap capacitor Cboot is equal to or lower than a predetermined voltage, charging of the bootstrap capacitor Cboot is performed by using the first charging control circuit 7, in a state in which the low side transistor Q2 is turned off. According to this, charging of the bootstrap capacitor Cboot is performed in much lower power consumption than charging the bootstrap capacitor Cboot by turning on the low side transistor Q2.

[0045]

In addition, when a voltage difference between the input voltage Vin and the output voltage Vout is equal to or lower than the first voltage, if the charged voltage of the bootstrap capacitor Cboot is equal to or lower than the second voltage, charging of the bootstrap capacitor Cboot is performed by turning of the low side transistor Q2, and thus the bootstrap capacitor Cboot can be quickly charged.

[0046]

While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

WHAT IS CLAIMED IS:

1. A DC-DC converter comprising:

a first transistor that is connected between a node of an input voltage and one terminal of an inductor;

a second transistor that is connected between the one terminal of the inductor and a reference voltage node;

a first gate control circuit that controls a gate voltage of the first transistor;

a capacitor that is connected between first and second power supplying nodes of the first gate control circuit;

a first detection circuit that detects whether or not a voltage difference between the input voltage and a voltage on the other terminal side of the inductor is equal to or lower than a first voltage; and

a first charging control circuit that, when the voltage difference is detected to be higher than the first voltage by the first detection circuit, if a charged voltage of the capacitor is equal to or lower than a predetermined voltage, charges the capacitor, in a state in which the second transistor is turned off.

2. The converter according to Claim 1, further comprising:

a second detection circuit which detects a voltage difference between a voltage on the other terminal side of the inductor and a reference output voltage that is set in advance;

a determination circuit that determines whether or not a load is in a light load state, based on the voltage difference detected by the second detection circuit;

a third detection circuit that detects whether or not a charged voltage of the capacitor is equal to or lower than a second voltage;

a second gate control circuit that, if it is determined by the determination circuit that the load is in the light load state, turns off the first transistor and the second transistor, and thereafter, if the charged voltage is detected to be equal to or lower than the second voltage by the third detection circuit and the voltage difference is detected to be equal to or lower than the first voltage by the first detection circuit, turns on the second transistor; and

a second charging control circuit that is connected between one terminal of the capacitor and the reference voltage node, and when the second transistor is turned on, charges the capacitor.

3. The converter according to Claim 1 or 2,

wherein, if a voltage difference between a node of the input voltage and the first power supplying node is higher than a predetermined voltage, the first charging control circuit includes a third transistor that charges the capacitor from the node of the input voltage via the first power supplying node.

4. The converter according to Claim 3,

wherein the first charging control circuit includes

a current source that is connected between the node of the input voltage and a gate of the third transistor; and

a constant voltage source that is connected between the gate of the third transistor and the second power supplying node.

5. The converter according to Claim 4,

wherein the constant voltage source is a Zener diode.

6. The converter according to any one of Claims 3 to 5,

wherein the third transistor operates at an active region.

7. The converter according to any one of Claims 1 to 4,

wherein, when the charged voltage is detected to be equal to or lower than the second voltage by the third detection circuit and the voltage difference is detected to be equal to or lower than the first voltage by the detection circuit, a period in which the first charging control circuit continuously charges the capacitor is longer than a period in which the second transistor is turned on.

ABSTRACT

According to one embodiment, a DC-DC converter includes a first transistor that is connected between a node of an input voltage and one terminal of an inductor; a second transistor that is connected between the one terminal of the inductor and a reference voltage node; a first gate control circuit that controls a gate voltage of the first transistor; a capacitor that is connected between first and second power supplying nodes of the first gate control circuit; a first detection circuit that detects whether or not a voltage difference between the input voltage and a voltage on the other terminal side of the inductor is equal to or lower than a first voltage; and a first charging control circuit that, when the voltage difference is detected to be higher than the first voltage by the first detection circuit, if a charged voltage of the capacitor is equal to or lower than a predetermined voltage, charges the capacitor, in a state in which the second transistor is turned off.

Drawings

FIG. 1

4: LOW VOLTAGE DETECTION CIRCUIT

11: LEVEL SHIFT CIRCUIT

5: VOLTAGE DIFFERENCE DETECTION CIRCUIT

6: LIGHT LOAD DETERMINATION CIRCUIT

13: SIGNAL PROCESSING UNIT

8: ERROR VOLTAGE DETECTION CIRCUIT

FIG. 3

CONSTANT VOLTAGE DETECTION CIRCUIT OUTPUT

FIG. 4

CONSTANT VOLTAGE DETECTION CIRCUIT OUTPUT

SECOND VOLTAGE